Deniz Gursoy

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EDUCATION

University of Pennsylvania, School of Engineering and Applied Science | Philadelphia, PA *August 2025 - May 2028 (Expected)*

Major: Electrical Engineering (Bachelor of Science in Engineering), *Minor:* Computer Science

Relevant Courses: Electrical Circuits & Systems + Electronic, Photonic & Electromechanical Devices + Signal Processing + Computer Architecture + Digital Logic Design (Verilog) + Power Electronics + Embedded Systems + Solid-State Circuits + Linear Algebra

PROFESSIONAL EXPERIENCE

SpaceX | Electrical & Controls Engineering Intern | Hawthorne, CA *May 2026 – August 2026*

- Designed, wired, and commissioned 4 industrial 480V control panels for a manufacturing program, writing custom PLC logic and EPLAN schematics for systems used to validate hardware ahead of Raptor engine production integration
- Supported cross-functional validation efforts before production, contributing to a 45% cost reduction and ~$75 million in savings
- Developed a PLC function-block system to replace a legacy alarm-handling process of 200+ fault codes

Syracuse University College of Engineering | Robotics Systems Engineering Intern | Syracuse, NY *June 2025 – August 2025*

- Created a custom hexacopter synthetic aperture radar platform by integrating a PulsON 440 radar with a Pixhawk flight stack and Raspberry Pi; Optimized powertrain to achieve 20% increase in flight stability during autonomous data collection
- Developed Python signal processing pipelines implementing backprojection and motion compensation, achieving sub-10cm resolution and a 40% reduction in image reconstruction latency

MIT Lincoln Labs | Beaver Works Autonomous Racecar Grand Prix Team Captain | Cambridge, MA *June 2023 – August 2023*

- Led a 5-student team to 1st place internationally, programming a 1/10-scale autonomous vehicle through a 9-section obstacle course with a LIDAR/IMU/OpenCV/PID autonomous stack achieving sub-100ms response and zero collisions

LEADERSHIP & ACTIVITIES

Penn Hyperloop | Controls Engineering Lead | Philadelphia, PA *September 2025 – Present*

- Upgraded 240V→480V three-phase AC system with 5+ VFDs controlling 15+ HP motors, enabling 300% greater power delivery for a 1,000-lb autonomous TBM that placed 2nd in The Boring Company's 2026 Not-a-Boring Competition
- Programmed Siemens S7-1200 PLC & ESP32 MCU with TIA Portal to implement autonomous drilling state machine with hardwired E-stops, software interlocks, and remote kill switch to ensure <100ms fail-safe response
- Integrated VFDs & sensors into unified HMI using Modbus RTU, I2C, and Ethernet protocols for synchronized telemetry

Penn Assistive Devices & Prosthetic Technologies | Project Co-Lead | Philadelphia, PA *September 2025 – Present*

- Developed 8-channel EMG acquisition system w/ 24-bit ADCs & programmable gain amplifiers for prosthetic arm control, with SPI-interfaced signal conditioning & dual voltage regulation (5V/3.3V), PCB schematics designed in Altium
- Transitioning from H-bridge linear actuator to dual-servo architecture to reduce mechanical complexity, while implementing modular Raspberry Pi Pico interface for rapid prototyping and user-specific calibration

Penn Institute of Electrical & Electronics Engineers (IEEE@Penn) | President | Philadelphia, PA *January 2026 – Present*

- Leading 100+ member student chapter; organizing technical panels, industry speaker events, and local competitions

RESEARCH

Modular Robotics Lab (GRASP Lab) | Undergraduate Research Assistant | Philadelphia, PA *February – September 2026*

- Designed capacitive sensing circuits (Schmitt trigger relaxation oscillator, OPA277 op-amp) for real-time joint angle detection

PROJECTS

Quadruped Learns to Walk with RL *June – July 2026*

- Trained a PPO locomotion policy for a simulated Unitree Go1 in MuJoCo, using domain randomization to achieve 100% recovery from 100N pushes and zero failures across 20 trials at 2× sensor noise

INT8 Systolic Array DNN Accelerator *July 2026*

- Designed and synthesized a weight-stationary systolic array (4×4, scaled to 8×8) in SystemVerilog for end-to-end INT8 MNIST inference, achieving 96.53% accuracy bit-exact against a PyTorch golden model and a 52× speedup over baseline at 65MHz on FPGA, with a custom visualizer built for RTL verification

TECHNICAL SKILLS

- Python, Java, C, C++, MATLAB, Linux, Altium, PLC, SOLIDWORKS, Git, ROS, TensorFlow, PyTorch, Reinforcement Learning, OpenCV, YOLO, FPGA, Modbus RTU, I2C, Verilog, OpenCL, OpenGL, CUDA, OpenMP, LTspice, VHDL